AMENDMENTS TO THE SPECIFICATION:

Please amend the title as follows:

--RAKE RECEPTION APPARATUS <u>HAVING ONE DELAY LOCK LOOP</u>

<u>CIRCUIT</u>--

Page 1, replace the paragraph beginning on line 11 and

bridging pages 1 and 2 with the following amended paragraph:

--In a spread spectrum communication system, a carrier

wave is modulated by transmission data and, in addition, the

carrier wave is multiplied with the pseudorandom noise (PN) code,

on the transmitting side, so that the carrier wave is transmitted

as it is modulated with the PN code and as the frequency spectrum

is spread. On the receiving side, the carrier wave is multiplied

with the same PN code as that used on the transmitting side. If

the PN code is the same PN code as and in phase with that used in

transmission, despreading occurs to produce a modulated output,

which is demodulated to derive reception data. In the spread

spectrum communication system, as discussed above, the received

signal is despread, so that the PN sequence which is the same as

that used on the transmitting side not only in pattern but also

in phase is needed. The code division multiple access (CDMA)

system enables multiple connection by changing the pattern and

the phase and is recently finding application in mobile

communication in that it is superior in interference ~~combatting~~

<u>combating</u> and intercept ~~combatting~~ <u>combating</u> performance and also

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in that it is able to realize reception characteristics that are optimal in a multi-path environment.--

Page 2, replace the paragraph beginning on line 4 with the following amended paragraph:

--In the CDMA-based mobile communication system, there is used a path diversity system (RAKE system) in which plural path signals are separately despread and demodulated by plural receivers ~~and plural path signals are separately despread and demodulated by plural receivers,~~ in order to reduce the effect of fading caused by the multipath propagation route and also in order to improve the signal-to-noise ratio.--

Page 6, replace the paragraph beginning on line 3 with the following amended paragraph:

--Fig. 2 shows a structure of a [[D11]] <u>DLL</u> circuit embodying the present invention.--

Page 6, replace the paragraph beginning on line 14 with the following amended paragraph:

--A preferred embodiment of the present invention is hereinafter explained. In the preferred embodiment of the present invention, a common one ~~display~~ <u>delay</u> lock loop (DLL) circuit is provided for plural finger circuits in a RAKE receiver, without providing a delay lock loop circuit (DLL circuit) for synchronization holding control for each finger circuit. The DLL circuit is caused by a changeover circuit to track an optimal finger circuit. The remaining finger circuits

are adapted for being controlled by clock outputs from the DLL circuit.--

Page 6, replace the paragraph beginning on line 23 and bridging pages 6 and 7 with the following amended paragraph:

--In more detail, the control circuit 3 controls the changeover circuit 4, based on the finger-based information, such as weighting information as found in ~~synthesising~~ synthesizing demodulated output signals of the respective finger circuits to select sequentially the finger circuits to be tracked by the DLL circuit 5.--

Page 8, replace the paragraph beginning on line 11 with the following amended paragraph:

--In a preferred embodiment of the present invention, the DLL circuit includes a PN sequence generator 60 for branching reception in-phase (I)/quadrature data (Q) input from [[th]] the finger circuit, for generating and outputting early PN codes (an in-phase component PNEI and a quadrature component PNEQ) earlier in frequency divider timing than the PN codes used in the finger circuit (an in-phase component PNI and a quadrature component PNQ) and for generating and outputting late PN codes (an in-phase component PNLI and a quadrature component PNLQ) later in frequency divider timing than the PN codes used in the finger circuit (PNI and PNQ);

a first complex multiplier 51 for multiplying the I/Q data with the PN codes (an in-phase component PNEI and a

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quadrature component PNEQ) generated by the PN sequence generator;

a second complex multiplier 54 for multiplying the I/Q data with the PN codes (PNLI, PNLQ) generated by the PN sequence generator;

a first low-pass filter 52 for smoothing an output of the first complex multiplier 51;

a second low-pass filter 55 for smoothing an output of the second complex multiplier 54;

a first amplitude detector 53 for detecting an output amplitude of the first low-pass filter;

a second amplitude detector 56 for detecting an output amplitude of the second low-pass filter;

a subtractor 57 for subtracting an output of the second amplitude detector 54 from an output of the first amplitude detector 53;

a loop filter 58 for smoothing an output of the subtractor 57; and

a voltage-controlled oscillator 59 fed with an output of the subtractor 57 as a control voltage; wherein

output clocks CK of the voltage-controlled oscillator 59 are routed to the PN sequence generator 60 and to the respective finger circuits (1, 6, 7, 8).--

Page 12, replace the paragraph beginning on line 15 with the following amended paragraph:

--~~Foe~~ <u>For</u> keeping the synchronization following initial acquisition, a DLL circuit 5 is used.--

Page 15, please replace the paragraph beginning on line 19 with the following amended paragraph:

--The input I/Q data, as received by ~~th~~ the finger circuit, is multiplied in the complex multiplier 51 with the PN code strings PNI, PNQ, so as to be output through a low-pass filter (LBF.) 12 to the RAKE combiner 2.--